Features

LVPECL, LVDS, HCMOS Output

5V, 3.3V Operation

Surface Mount Package

Tri-state

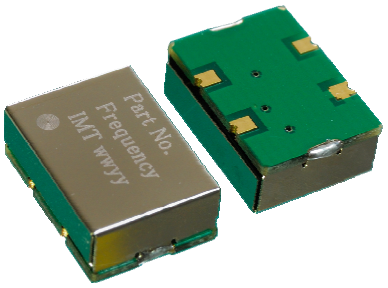
AT-Cut Crystal

Fund, 3rd Oscillation Mode.

0to70℃, -40to85℃ OPT Range.

Low RMS Phase Jitter

RoHS Compliant (pb-Free)



Dimensions(mm) **14.2 x 10.2 x 5.2max**

Absolute Maximum Ratings(*For user guidelines only*)

Parameter	Maximum Value	Units	Condition
Supply voltage(Vdd)	6	Vdc	
Operating Temperature	-40 to 85	℃	
Storage Temperature	-50 to 120	℃	Max
ESD Sensitivity	1	kV	HBM

Supply Voltage & Consumption.

Parameter	Value	Units	Condition
Supply Voltage(Vdd)	3.3V ±5%	DC	
Current Consumption	30	mA Max	HCMOS
	25	mA Max	LVDS
	85	mA Max	LVPECL
Supply Voltage(Vdd)	5.0V ±5%	DC	
Current Consumption	40	mA Max	HCMOS
	120	mA Max	LVPECL
Start up Time(Ts)	5	mS	Max

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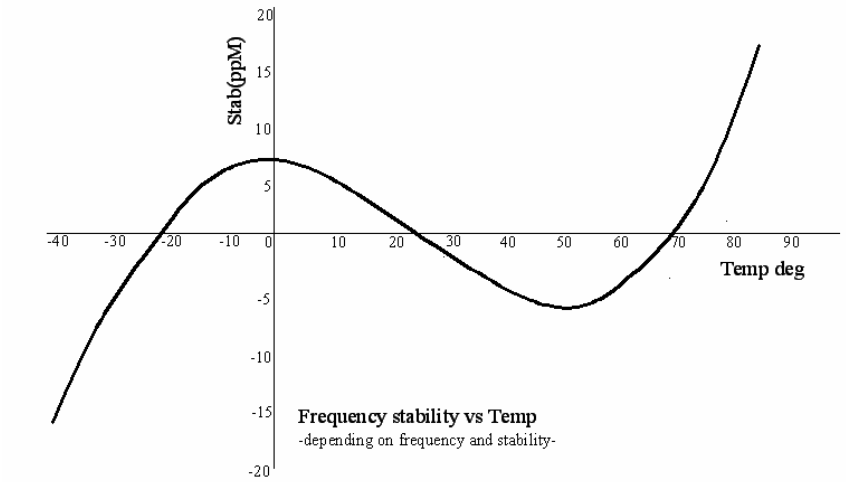
Frequency Stabilities[1]

Parameter	Typical Value	Units	Condition
Vs. Temperature	±10 ±25	ppM max ppM max	0to70℃ -40to85℃
Vs. Calibration @25℃	±10	ppm max	±2℃
Vs. Vdd	±1	ppm max	±5% of Vdd
Vs. Load	±0.3	ppM max	±5% change
Aging 1st year	±2	ppM max	
Overall Stability (includes temperature And initial accuracy)	±15 ±25 ±50	ppM max ppM max ppM max	0to50℃ -20to70℃ -40to85℃



Frequency stability vs Temp
-depending on frequency and stability-

RF output[1]

	Parameter	Typical Value	Units	Condition
HCMOS	Output Load	15	pF	
	Rise(Tr),Fall(Tf) time	10	nS max	10to 90%
	Output Level High	10%Vdd	V min	VOH
	Output Level Low	90%Vdd	V max	VOL
	Symmetry	50±10	%	50% of Vdd
LVPECL	Output Load	50 ohm into Vdd-2.0Vdc		
	Rise(Tr),Fall(Tf) time	1	nS max	20to 80%
	Output Level High	Vdd-1.025	V min	VOH

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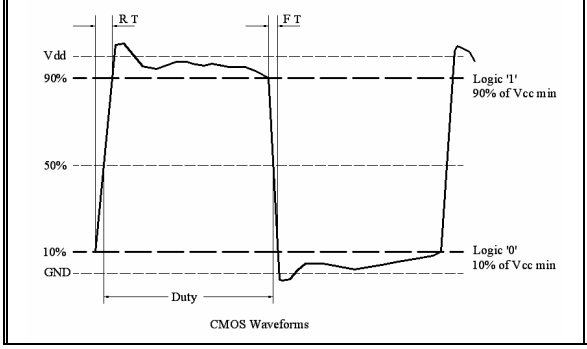
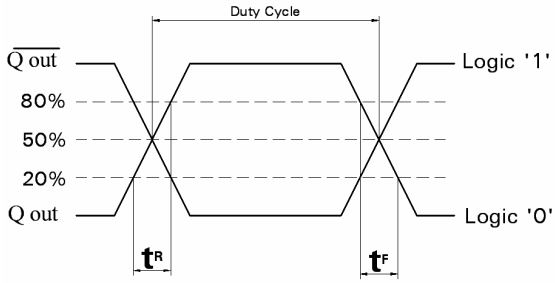
	Output Level Low	Vdd-1.62	V max	VOL
	Symmetry	50±10	%	50% of Vdd
1 About Test Condition Refer to Wave Form				

Wave Form

HCMOS

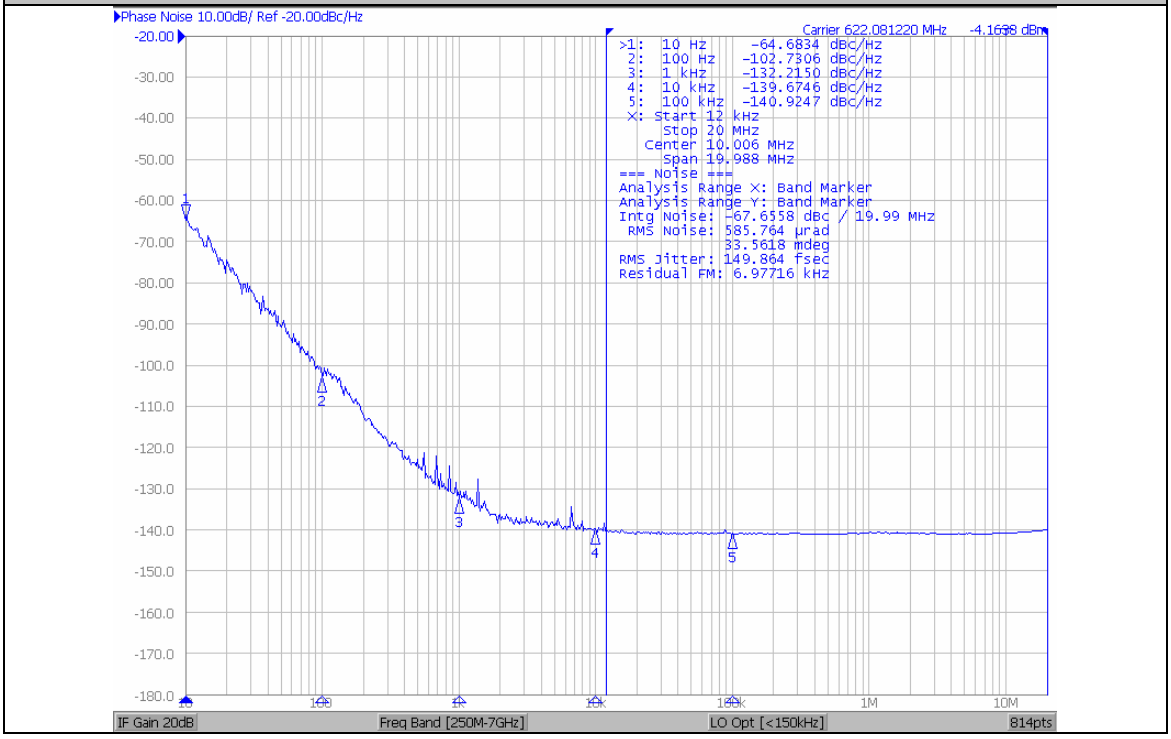


LVPECL & LVDS

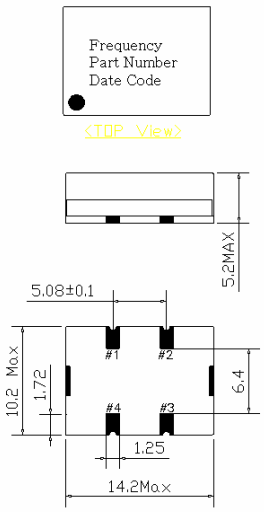
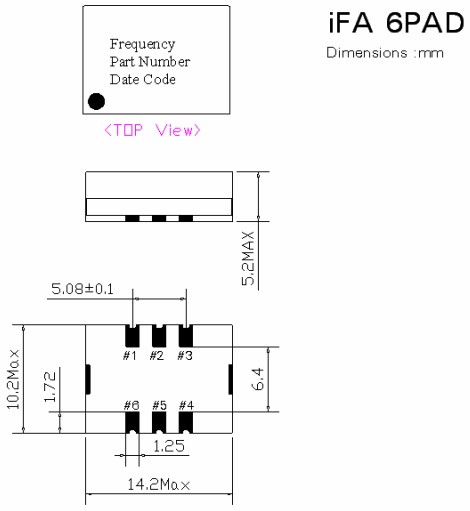


Phase Noise

iXPFA3 622M080



Mechanical Dimensions

FA 4PAD for HCMOS	FA 6PAD for PECL,HCMOS,LVDS
	
Code:FA4 Dimensions: 14 X 10 X 5.2	Code:FA6 Dimensions: 14 X 10 X 5.2

Pin Connections	Pin Connection
Pin1 : N/C or E/D Pin2 : Ground Pin3 : Output Pin4 : supply voltage(Vdd)	Pin1: N/C or E/D Pin2: N/C Pin3: Ground Pin4: Output(Q) Pin5: Complementary Output($\bar{Q}$) (for PECL and LVDS) Pin6 : supply Voltage(Vdd)

TRUTH TABLE	HCMOS		LVPECL,LVDS	
Pin1	Q	$\bar{Q}$	Q	$\bar{Q}$
"1"Level	Data	N.C	H.I	H.I
"0"Level	High	N.C	Data	Data
N/C	Data	N.C	Data	Data
N/C : No Connect, H.I: High impedance.				

Marking

156.250Mhz	-Frequency
iXPFA3-EC0	-Part No.
• IMT wwyy	-week/year

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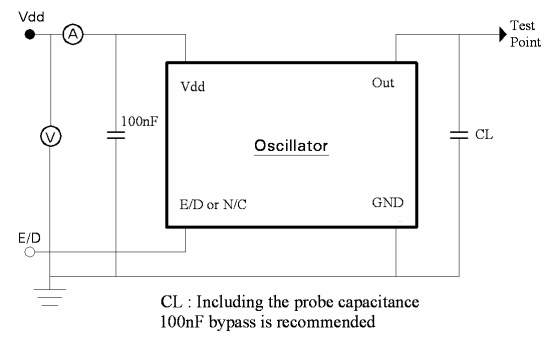
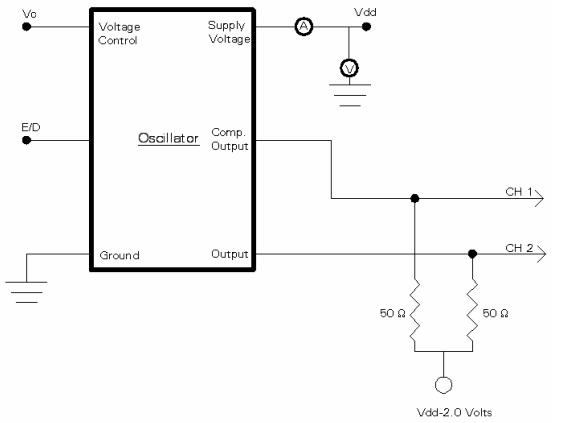
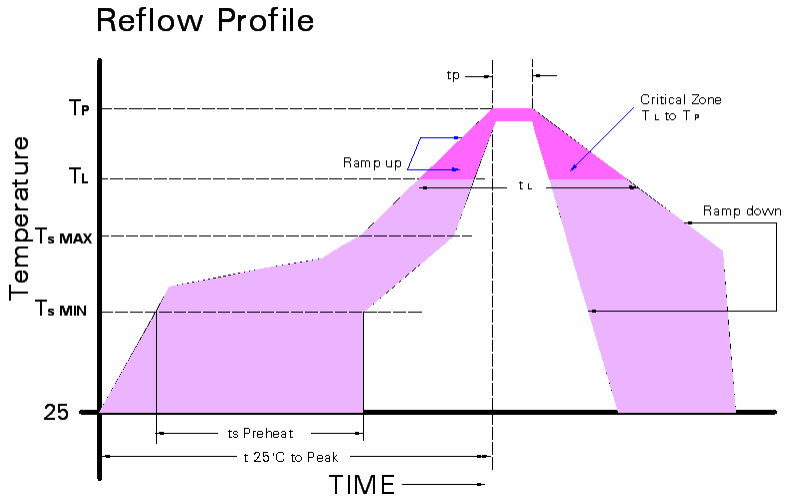
Load Configuration

HCMOS	LVPECL
	

Note : Recommend to add 100nF bypass Capacitors at Vdd and Vc

Recommended Reflow Profile



Note: Temperatures refer to body of device.
Oscillators must be on the top side of the PCB during the reflow process.

Ts max to TL (Ramp-up rate)	3℃/second max
Preheat –Temperature Min(Ts min) -Temperature Typical(Ts TYP) -Temperature Max(Ts Max) -Time(ts)	150℃ 175℃ 200℃ 60-180 Seconds
Ramp-up Rate(TL to TP)	3℃/Second max
Time Maintained Above-Temperature(TL) -Time(TL)	217℃ 60-150 Seconds

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Peak Temperature(Tp)	260℃ Max for 10 seconds Max
Target Peak Temperature(Tp Target)	250℃
Time within 5℃of actual peak(tp)	20-40 seconds
Ramp-down Rate	6℃/second max
Time 25℃ to peak Temperature	8 minutes max

Part Numbering Guide & Code …iXPFA3-EC0-156M250-T

iX*P*FA (LVPECL)

Logic	Supply voltage	Operating Temperature	Stability	Frequency	Packaging Option
iX*P*FA	3	E	C0	156M250	T
P: LVPECL H: HCMOS L: LVDS	5:5.0V 3:3.3V	A: 0…50℃ B: 0…70℃ E:-40…85℃	A5: ±15ppM B5: ±25ppM E0: ±50ppM	156.250Mhz	T: Tape & Reel B: Bulk
Above example, Crystal Oscillator, PECL output, SMD package, 3.3V, -40to 85℃ Temperature range, Overall ±25ppM, at 156.250Mhz.					

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