Clipped Sine, CMOS 14pin-Dip TCXO | Freq : 1Mhz to 64Mhz

Features

Temperature Compensated Crystal Oscillator

5V, 3.3V Operation

Adjustable Frequency

HCMOS Output or Clipped Sine output

AT-Cut Crystal

Fund, 3rd Oscillation Mode.

-20to70℃, -40to85℃ OPT Range.

Low RMS Phase Jitter

RoHS Compliant (pb-Free)

Dimensions(mm) 20.8 x 13.2 x 7.0max

Typical Applications

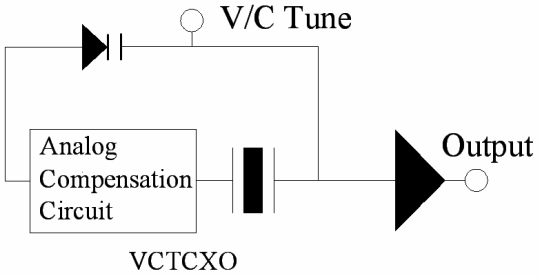
Base Station

Test Equipment

Any application requiring an VCTCXO,TCXO

Cellular Telephony

Block Diagram



VCTCXO

Vc must be applied to Pin #1 on VCTCXO's

Absolute Maximum Ratings(*For user guidelines only*)

Parameter	Maximum Value	Units	Condition
Supply voltage(Vdd)	7	Vdc	
Operating Temperature	-40 to 85	℃	
Storage Temperature	-50 to 120	℃	Max
ESD Sensitivity	1	kV	HBM

Supply Voltage & Consumption.

Parameter	Value	Units	Condition
Supply Voltage(Vdd)	5.0V ±5%	DC	
Current Consumption	15	mA Max	Clipped sine
	50	mA Max	CMOS

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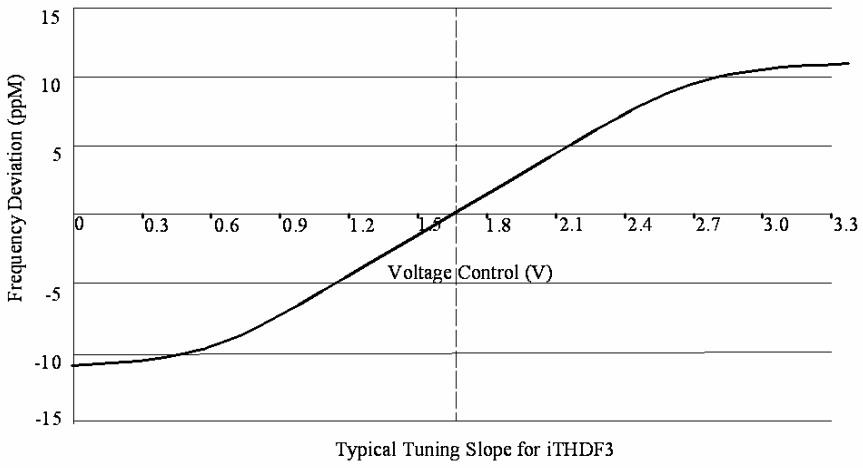
Supply Voltage(Vdd)	3.3V ±5%	DC	
Current Consumption	10	mA Max	Clipped sine
	30	mA Max	CMOS
Start up Time(Ts)	5	mS	Max

Frequency Tuning(Vc) - Option

Parameter	Typical Value	Units	Condition
Vc. Turning Range	0.3 to 3.0	V	Vdd 3.3V
	0.5 to 4.5	V	Vdd 5.0V
Electrical Tuning	±10	ppM min	Standard[1]
Internal Trimmer	±3	ppM min	Mechanical
Linearity	±10.0	%	Max
NorminalCenterVoltage	50%of Vdd[1]	V	
Input impedance	10	Kohm	Min
Tuning slope	Positive		

[1] Other Tuning Range is also available on customer specification.



Typical Tuning Slope for iTHDF3

Frequency Stabilities[1]

Parameter	Typical Value	Units	Condition
Vs. Temperature[2]	±1.0	ppM max	0to70℃
	±2.0	ppM max	-20to70℃
	±3.0	ppM max	-40to85℃

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Vs. Calibration @25℃	±1.0	Ppm max	±2℃
Vs. Vdd	±0.2	ppm max	±5% of Vdd
Vs. Load	±0.2	ppM max	±5% change
Aging 1st year	±1.0	ppM max	
[1] Vc. condition is 50% of Vdd. [2] Other Stability and Temperature range available.			

RF output[1]

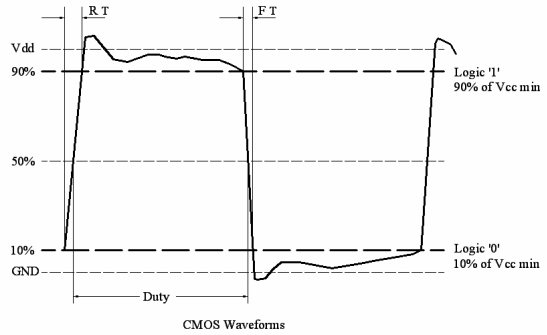
Parameter		Typical Value	Units	Condition
HCMOS	Output Load	15	pF	
	Output Voltage(VOH)	90% of Vdd	V min	
	(VOL)	10% of Vdd	V max	
	Rise(Tr),Fall(Tf) time	5	nS max	10to 90%
	Symmetry	50±10	%	50% of Vdd
SINE	Output Load[2]	10	Kohm	
	Output Power	0.8	Vpp min	10Kohm//10pF

[1] About Test Condition Refer to Wave Form

[2] 50 Ohm Load is also available.

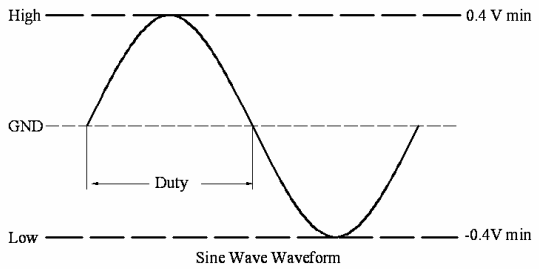
Wave Form

HCMOS



CMOS Waveforms

Clipped Sine & Sine



Sine Wave Waveform

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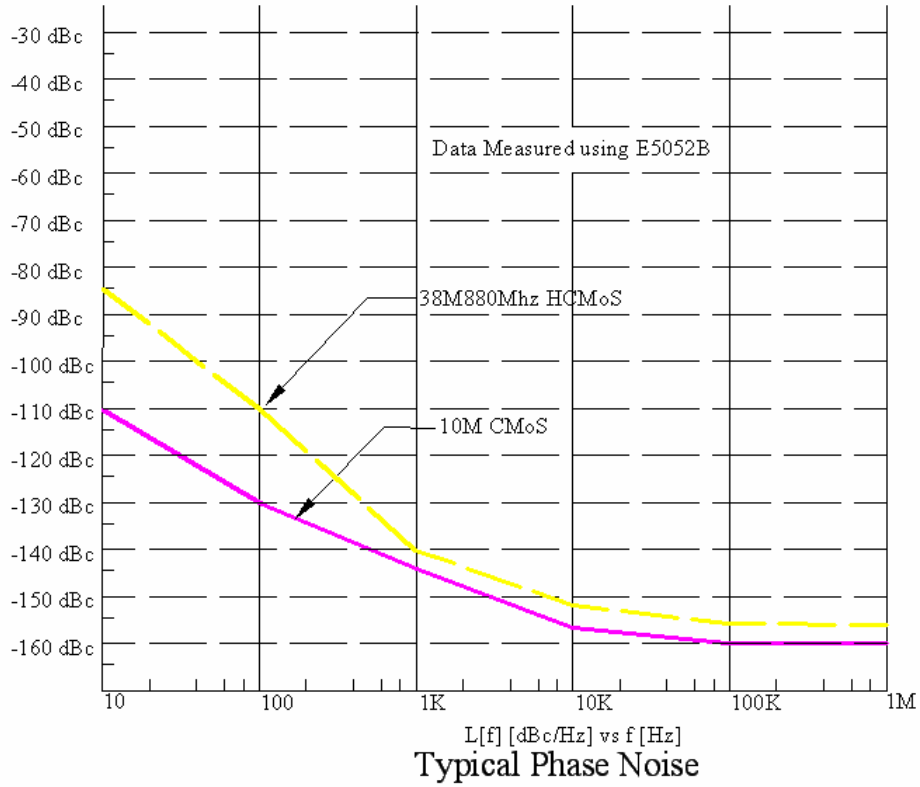
Phase Noise

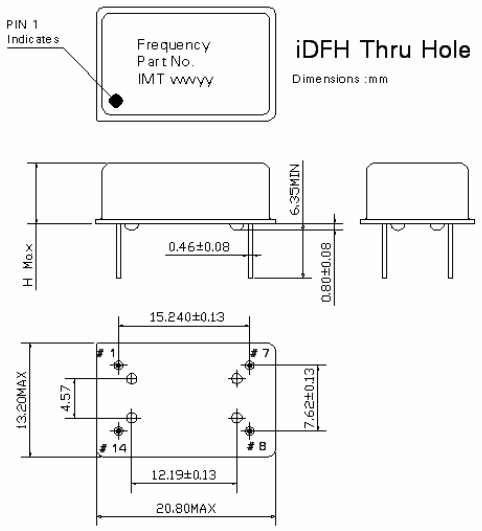
iTTDF5 10M000, iTTDF5 38M880



Typical Phase Noise

Mechanical Dimensions

DF 14pin Thru-Hole	Pin Connection



Pin1 : Voltage Control(Vc) or N/C, Tri-state
Pin2 : Ground
Pin3 : Output
Pin4 : supply voltage(Vdd)

Code: DFH	Dimensions: 20.8 X 13.2 X 7.0

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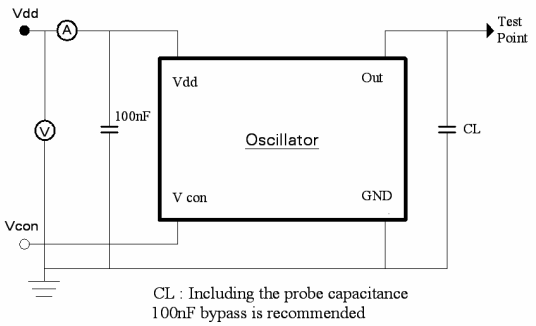
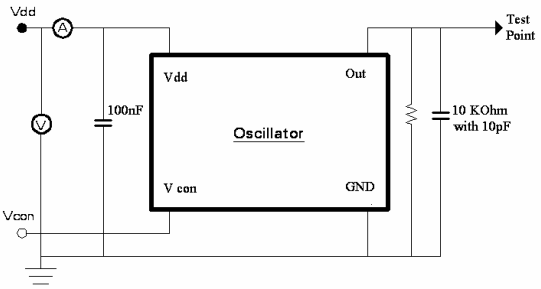
Marking

10.000Mhz	-Frequency
iTTDF5-B10	-Part No.
• IMT wwyy	-week/year

Load Configuration

HCMOS	Clipped Sine wave
	

Note : Recommend to add 100nF bypass Capacitors at Vdd and Vc

Part Numbering Guide & Code …iTTDF5-B10-10M000-T

iT*H*DF (HCMOS)[1]

iT*C*DF (Clipped Sinewave)

Logic	Supply voltage	Operating Temperature	Stability	Frequency	Packaging Option
iT*H*DF	5	B	10	10M000	T
C: SINE H: HCMOS L: LVDS	5:5.0V 3:3.3V	B: 0…70℃ C:-20…70℃ E:-40…85℃	10: ±1.0ppM 25: ±2.5ppM 30: ±3.0ppM	10.000Mhz	T: Tape & Reel B: Bulk

Above example, TCXO, CMOS output, Dip14 package, 5.0V, -20to 70℃ Temperature range, Temp Stability ±1.0ppM, at 10.000Mhz.

iW*H*DF (HCMOS)[2]

iW*C*DF (Clipped Sinewave)

Logic	Supply voltage	Operating Temperature	Stability	Frequency	Packaging Option
iW*H*DF	5	B	10	10M000	T
C: SINE H: HCMOS L: LVDS	5:5.0V 3:3.3V	B: 0…70℃ C:-20…70℃ E:-40…85℃	10: ±1.0ppM 25: ±2.5ppM 30: ±3.0ppM	10.000Mhz	T: Tape & Reel B: Bulk

Above example, VCTCXO, CMOS output, Dip14 package, 5.0V, -20to 70℃ Temperature range, Temp Stability ±1.0ppM, at 10.000Mhz.

[1] iT meaning a Temperature Compensation Crystal Oscillator.

[2] iW meaning a Voltage Controlled TCXO, has EFC.

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